CLAIMS

1. An integrated circuit package assembly for electrically isolating modules, comprising:

a substrate having a first side and an opposing second side;

a first module attached to the first side of the substrate;

a second module attached to the first side of the substrate;

a first conductive surface proximate to the second side of the substrate, the first conductive surface conductively coupled to the first module; and

a second conductive surface spaced apart from the first conductive surface to form a capacitor with the first conductive surface, the second conductive surface being coupled to the second module.

2. The package assembly of claim 1, further comprising a dielectric interposed between the first and second conductive surfaces.

3. The package assembly of claim 1, further comprising an encapsulation substantially surrounding the package assembly.

4. The package assembly of claim 3 wherein the package assembly is encased in a polymer.

5. The package assembly of claim 3 wherein the package assembly is encased in ceramic.

6. The package assembly of claim 3 wherein the package assembly is encased in a glass.

7. The package assembly of claim 1 wherein the first module is an integrated circuit.

8. The package assembly of claim 7 wherein the integrated circuit is a physical layer chip.

9. The package assembly of claim 1 wherein the second module is an integrated circuit.

10. The package assembly of claim 9 wherein the integrated circuit is a link layer chip.

11. The package assembly of claim 1, further comprising a resistor having a first terminal coupled to the first conductive surface and further having a second terminal coupled to the second conductive surface.

12. The package assembly of claim 10 wherein the resistor has a resistance of approximately one megohm.

13. The package assembly of claim 11 wherein the resistor is a resistant film.

14. The package assembly of claim 1, further comprising a first ground plane connected to the first conductive surface, and a second ground plane connected to the second conductive surface.

15. The package assembly of claim 13 wherein the first ground plane comprises a ground wire of a cable bus.

16. The package assembly of claim 13 wherein the second ground plane comprises a chassis of a computer.

17. An integrated circuit package assembly for electrically isolating integrated circuits within a module, comprising:

a substrate having a first side and an opposing second side;

a module attached to the first side of the substrate, the module having a first and second integrated circuit;

a first conductive surface proximate to the second side of the substrate, the first conductive surface conductively coupled to the first integrated circuit; and

a second conductive surface spaced apart from the first conductive surface to form a capacitor with the first conductive surface, the second conductive surface being conductively coupled to the second integrated circuit.

18. The package assembly of claim 16, further comprising a dielectric interposed between the first and second conductive surfaces.

19. The package assembly of claim 16, further comprising an encapsulation substantially surrounding the package assembly.

20. The package assembly of claim 18 wherein the package assembly is encased in a polymer.

21. The package assembly of claim 18 wherein the package assembly is encased in ceramic.

22. The package assembly of claim 18 wherein the package assembly is encased in a glass.

23. The package assembly of claim 16 wherein the first module is an integrated circuit.

24. The package assembly of claim 22 wherein the integrated circuit is a physical layer chip.

25. The package assembly of claim 16 wherein the second module is an integrated circuit.

26. The package assembly of claim 24 wherein the integrated circuit is a link layer chip.

27. The package assembly of claim 16, further comprising a resistor having a first terminal coupled to the first conductive surface and further having a second terminal coupled to the second conductive surface.

28. The package assembly of claim 26 wherein the resistor has a resistance of approximately one megohm.

29. The package assembly of claim 27 wherein the resistor is a resistant film.

30. The package assembly of claim 16, further comprising a first ground plane connected to the first conductive surface, and a second ground plane connected to the second conductive surface.

31. The package assembly of claim 28 wherein the first ground plane comprises a ground wire of a cable bus.

32. The package assembly of claim 28 wherein the second ground plane comprises a chassis of a computer.

33. An integrated circuit package assembly for electrically isolating modules, comprising:

a first substrate with a first and opposing second side having a first module attached to the first side;

a first conductive surface proximate to the second side of the first substrate, the first conductive surface being conductively coupled to the first module;

a second substrate with a first and opposing second side having a second module attached to the first side; and

a second conductive surface proximate to the opposing side of the second substrate, the second conductive surface being conductively coupled to the second module and spaced apart from the first conductive surface to form a capacitor with the first conductive surface.

34. The package assembly of claim 31, further comprising a dielectric interposed between the first and second conductive surfaces.

35. The package assembly of claim 31, further comprising an encapsulation substantially surrounding the package assembly.

36. The package assembly of claim 33 wherein the package assembly is encased in a polymer.

37. The package assembly of claim 33 wherein the package assembly is encased in ceramic.

38. The package assembly of claim 33 wherein the package assembly is encased in a glass.

39. The package assembly of claim 31 wherein the first module is an integrated circuit.

40. The package assembly of claim 37 wherein the integrated circuit is a physical layer chip.

41. The package assembly of claim 31 wherein the second module is an integrated circuit.

42. The package assembly of claim 39 wherein the integrated circuit is a link layer chip.

43. The package assembly of claim 31, further comprising a resistor having a first terminal coupled to the first conductive surface and further having a second terminal coupled to the second conductive surface.

44. The package assembly of claim 41 wherein the resistor has a resistance of approximately one megohm.

45. The package assembly of claim 43 wherein the resistor is a resistant film.

46. The package assembly of claim 31, further comprising a first ground plane connected to the first conductive surface, and a second ground plane connected to the second conductive surface.

47. The package assembly of claim 43 wherein the first ground plane comprises a ground wire of a cable bus.

48. The package assembly of claim 43 wherein the second ground plane comprises a chassis of a computer.

49. An integrated circuit package assembly for electrically isolating integrated circuits within a module, comprising:

a substrate;

a first module having a first and opposing second side attached to the substrate on the first side;

a second module having a first and opposing second side attached to the substrate on the first side;

a non-conductive layer having a first and opposing second side, the first side proximate to the opposing second sides of the first and second modules;

a first conductive surface proximate to the second side of the first non-conductive layer, the first conductive surface conductively coupled to the first module; and

a second conductive surface spaced apart from the first conductive surface to form a capacitor with the first conductive surface, the second conductive surface being conductively coupled to the second module.

50. The package assembly of claim 46, further comprising a dielectric interposed between the first and second conductive surfaces.

51. The package assembly of claim 46, further comprising an encapsulation substantially surrounding the package assembly.

52. The package assembly of claim 48 wherein the package assembly is encased in a polymer.

53. The package assembly of claim 48 wherein the package assembly is encased in ceramic.

54. The package assembly of claim 48 wherein the package assembly is encased in a glass.

55. The package assembly of claim 46 wherein the first module is an integrated circuit.

56. The package assembly of claim 52 wherein the integrated circuit is a physical layer chip.

57. The package assembly of claim 46 wherein the second module is an integrated circuit.

58. The package assembly of claim 54 wherein the integrated circuit is a link layer chip.

59. The package assembly of claim 46, further comprising a resistor having a first terminal coupled to the first conductive surface and further having a second terminal coupled to the second conductive surface.

60. The package assembly of claim 56 wherein the resistor has a resistance of approximately one megohm.

61. The package assembly of claim 59 wherein the resistor is a resistant film.

62. The package assembly of claim 46, further comprising a first ground plane connected to the first conductive surface, and a second ground plane connected to the second conductive surface.

63. The package assembly of claim 58 wherein the first ground plane comprises a ground wire of a cable bus.

64. The package assembly of claim 58 wherein the second ground plane comprises a chassis of a computer.

65. An integrated circuit package assembly for electrically isolating modules, comprising:

a substrate having a first side and an opposing second side;

a first module having a first and opposing second side attached to the first side of the substrate on the first side of the first module;

a second module attached to the second side of the first module;

a first conductive surface proximate to the second side of the substrate, the first conductive surface conductively coupled to the first module; and

a second conductive surface spaced apart from the first conductive surface to form a capacitor with the first conductive surface, the second conductive surface being coupled to the second module.

66. The package assembly of claim 61, further comprising a dielectric interposed between the first and second conductive surfaces.

67. The package assembly of claim 61, further comprising an encapsulation substantially surrounding the package assembly.

68. The package assembly of claim 63 wherein the package assembly is encased in a polymer.

69. The package assembly of claim 63 wherein the package assembly is encased in ceramic.

70. The package assembly of claim 63 wherein the package assembly is encased in a glass.

71. The package assembly of claim 61 wherein the first module is an integrated circuit.

72. The package assembly of claim 67 wherein the integrated circuit is a physical layer chip.

73. The package assembly of claim 61 wherein the second module is an integrated circuit.

74. The package assembly of claim 69 wherein the integrated circuit is a link layer chip.

75. The package assembly of claim 61, further comprising a resistor having a first terminal coupled to the first conductive surface and further having a second terminal coupled to the second conductive surface.

76. The package assembly of claim 71 wherein the resistor has a resistance of approximately one megohm.

77. The package assembly of claim 75 wherein the resistor is a resistant film.

78. The package assembly of claim 61, further comprising a first ground plane connected to the first conductive surface, and a second ground plane connected to the second conductive surface.

79. The package assembly of claim 73 wherein the first ground plane comprises a ground wire of a cable bus.

80. The package assembly of claim 73 wherein the second ground plane comprises a chassis of a computer.

81. A method of electrically isolating modules within an integrated circuit package assembly, comprising:

attaching a first and second module to a substrate having a first and opposing second side;

providing a first conductive surface having a first and opposing second side abutting the opposing second side of the substrate;

providing a dielectric layer having a first and opposing second side abutting the opposing second side of the first conductive surface;

providing a second conductive surface abutting the opposing second side of the dielectric;

conductively coupling the first conductive surface to the first module; and

conductively coupling the second conductive surface to the second module.

82. The method of claim 76, further comprising encasing the assembly in a polymer.

83. The method of claim 76, further comprising encasing the assembly in a ceramic.

84. The method of claim 76, further comprising encasing the assembly in glass.

85. A method of electrically isolating modules within an integrated circuit package assembly, comprising:

forming a capacitor within the semiconductor package assembly, the capacitor having a first terminal and a second terminal;

coupling a first module to the first terminal of the capacitor; and

coupling a second module to the second terminal of the capacitor.

86. The method of claim 80 wherein the capacitor is formed proximate to a second side of a substrate having a first and opposing second side upon which the modules are attached.

87. The method of claim 81, wherein the modules are attached to the first side of the substrate and the capacitor is formed proximate to the second side of the substrate.

88. The method of claim 80, wherein the modules have first and opposing second sides and are attached to a substrate on the first sides of the modules and the capacitor is formed proximate to the opposing second sides of the modules.

89. The method of claim 80, wherein the capacitor is formed between a first module attached to a first substrate and a second module attached to a second substrate.